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# Contents

# Study on Ferroelectric Properties of $TiO_2$ / $SiO_2$ /p-Si (Metal/ Ferroelectric/ Insulator/Semiconductor) Thin Films

May Yee Thein[1], Yin Yin Thein[2], Than Than Win[3] and Ko Ko Kyaw Soe[4]

## Abstract

Fabrication of $TiO_2/SiO_2$/p-Si (Metal/ Ferroelectric/ Insulator/ Semiconductor) thin films, deposited by liquid phase epitaxial growth method is presented. Samples are heated at 500°C, 550°C, 600°C, 650°C and 700°C each for 1hr respectively. The ferroelectric properties such as the remanent polarization $P_r$, the spontaneous polarization $P_s$, the coercive field $E_C$ and the memory window (MW) of thin films are studied.

**Keywords**: remanent polarization, spontaneous polarization, coercive field, memory window .

## Introduction

Ferroelectric materials can be used in different ways in memory designs. The first used is a thin film of ferroelectric in a capacitor as a nonvolatile storage element using the hysteresis property of polarization versus voltage as the means of storing data. $TiO_2$ is well known as a fundamental ferroelectric oxide. Titania ($TiO_2$) has excellent in optical, dielectric and catalytic properties and is widely used in industry. Anatase phase $TiO_2$ plays an important role in solving various environmental problems because it can destroy harmful contaminants in water soil and air. Compared to other photocatalysts, titania is cheaper and nontoxic to human body and thus, is commercialized as the most powerful photocatalyst due to its high efficiency and wide applications in most photocatalytic reactions.

Thin films are fabricated by the deposition of individual atoms on a substrate. Their thickness is typically less than several microns. Thin films are now widely used for making electronic devices, optical coatings and decorative parts. Ferroelectric thin films have been attracting a great deal of attention because of their potential application in microelectronic and micro mechanical field. As modern electronic devices, such as mobile phones and note book computers, become popular, considerable attention is focused on ferroelectric devices, particularly non volatile memory devices.

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Ferroelectric random access memories (Fe RAM) have good features such as high speed operation, low power consumption, and large scale integration (LSI). A number of efforts have been undertaken to prepare good ferroelectric thin films by various methods such as RF sputtering, electron beam evaporation, ion beam sputtering, metal organic chemical vapor deposition, laser ablation and sol-gel processing. An insulating buffer layer is usually inserted between the ferroelectric material and Si. Such a structure is called a MFIS (Metal/ Ferroelectric /Insulator/ Semiconductor).

An important characteristic of ferroelectric is the ferroelectric hysteresis loop. A ferroelectric hysteresis loop can be observed by means of a Sawyer-Tower circuit. Circuit arrangement of P-E measurement with Sawyer-Tower circuit was shown in Fig 2. The external bias applied to the circuit is saw tooth wave of frequency 100 kHz. In a ferroelectric material, on the other hand, there is a spontaneous polarization, a displacement which is inherent to the crystal structure of the material and does not disappear in the absence of the electric field. In addition, the direction of this polarization can be reversed or reoriented by applying an appropriate electric field. The best ferroelectric properties (high remnant polarization and low coercive field) are found for epitaxial films. The P-E characteristic, remnant polarization versus bias voltage, and remnant polarization versus frequency of $TiO_2/SiO_2$/p-Si thin film are studied using the Sawyer-Tower circuit.

The purpose of this paper is to investigate the processing conditions for preparation of MFIS structures using ferroelectric $TiO_2$ thin films and $SiO_2$ as buffer layers. The hysteresis loops measured from Sawyer-Tower technique shows the behavior of nonvolatile memory.

## Experimental Procedure

$TiO_2$ powder materials (purity 99.99%) are placed in cleaned beaker. The 2-methoxyethanol ($CH_3OCH_2CH_2OH$) solvent is added in $TiO_2$ powder and stirred with glass stirrer thoroughly till these are homogenous. The mixture solution is stirred and heated up to 100°C by using indirect heat treatment. After heat treatment, the solution is cooled down to room temperature. Finally, the precursor solution or coating solution is obtained. The p-Si (100) wafer of dimension 0.5cmx0.5cm and thickness 625μm are used as substrate. Then silicon substrates are cleaned in acetone for 5min and dried in air atmosphere. Then they are rinsed with DW (distilled water) for a few minutes and dried at room temperature. To form MFIS structure, the $SiO_2$ , buffered layer is grown on cleaned p-Si substrate by thermal oxidation and the precursor solution of $TiO_2$ is deposited on $SiO_2$ /p-Si substrate by spin coating. After the spin coating process, the $TiO_2$ layer deposited on $SiO_2$ / p-Si films are annealed at 500°C, 550°C, 600°C ,650°C,700°C for one hour. For electrical measurements, Ag electrodes are used. The schematic representation of $TiO_2$ films deposited on $SiO_2$ / p-Si substrate is shown in Fig 1.

## Results and Discussion

The polarization versus electric field characteristics of the ferroelectric thin films is investigated to determine the hysteresis parameters. The P-E hysteresis loop display on oscilloscope by using Sawyer- Tower circuit are shown in Fig 3(a ~ e). The changes of remnants polarization $P_r$ and coercive field $E_c$ are investigated from the hysteresis loop measurements. The voltage $v_{pp}$= 10V with frequency 100 kHz is applied to the circuit. The variation of remnant polarization $2P_r$ with applied bias voltage is observed. Fig 4 represents the saturations properties of $TiO_2/SiO_2$ /p-Si thin films with Ag electrodes. From the saturation plot, the value of $2P_r$ is linearly increased in applied voltage and it reaches to saturate state. The working voltage is examined to be 5.5 V for all fabricated films.

Fig 5 represents the dispersion of hysteresis parameters such as $P_r$, $P_s$ and $E_c$ as a function of substrate temperatures. According to that figure remnant polarization gradually increases with increasing bias voltage, which is consistent with theory of ferroelectricity. It is obvious that the largest value of $P_r$ is caused by the film at 700°C. The minimum coercive value is occurred the $TiO_2$ cell at 550°C. Fig 6 shows the memory window versus process temperature of $TiO_2$ thin films at 10V. The memory window is linearly increased with increasing the process temperature is shown in Fig 6. The widest memory window is found at the fabricated memory cell at 600°C.

## Conclusion

Growth of Ag/ $TiO_2$ / $SiO_2$ /p-Si thin film and its memory behavior have been successfully investigated. Processing parameters are systematically observed in this study. All fabricated films are examined to be ferroelectrics because of the formation of nonlinear P-E hysteresis loop. Slim, symmetric and norminal saturating hysteresis loop is formed by the cell at 600°C for Ag/$TiO_2$ /$SiO_2$ /p-Si thin film. The polarization is reached its maximum value (1) when absence of electric field (0) whereas the value of polarization is approached zero (0) when the maximum field (1) applied. Thus, the fabricated cells are utilized for non-volatile memory device. Working voltage of all fabricated cells is found to be 5.5V. According to the experimental results all hysteresis parameters are found in accepted range for non- volatile memory technology. The present results in this research indicate our fabricated MFIS multilayer memory devices with new sol-based method are quite promising candidates for memory device application.

## Acknowledgement

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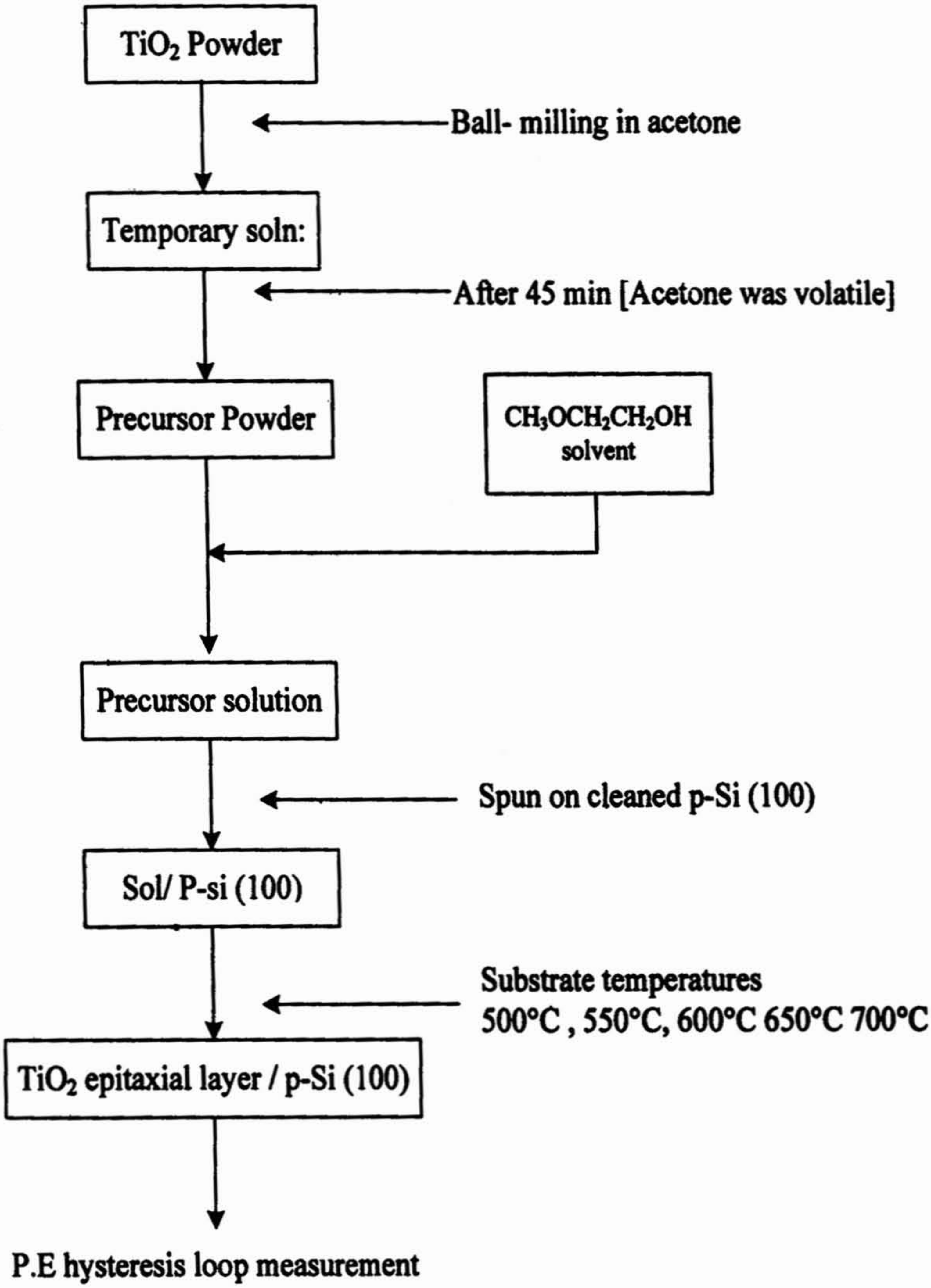


Fig 1 Schematic representation of $TiO_2$ formed $SiO_2$ /p-Si (100)

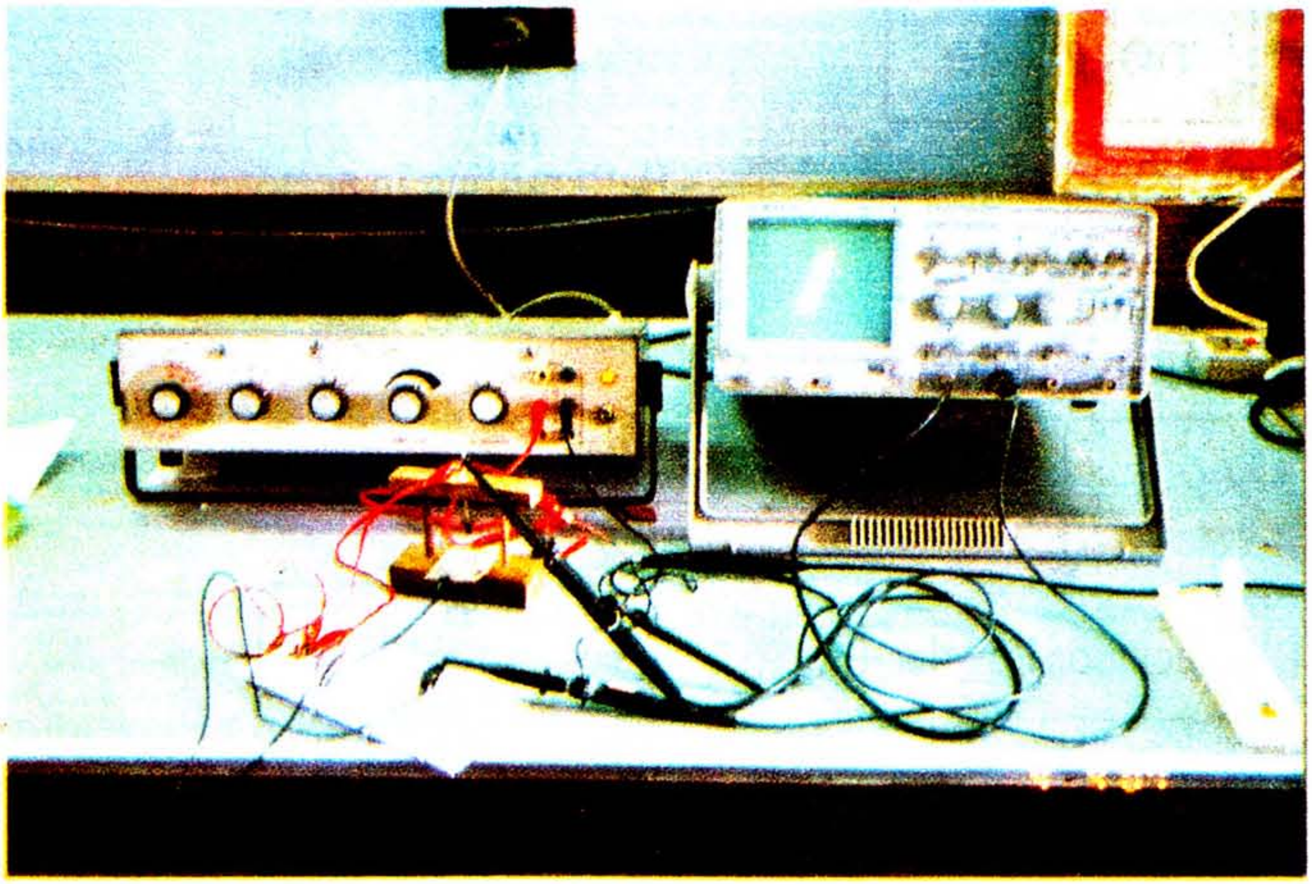

Fig. 2. Circuit arrangement of Sawyer-Tower circuit foP-E Measurement in laboratory

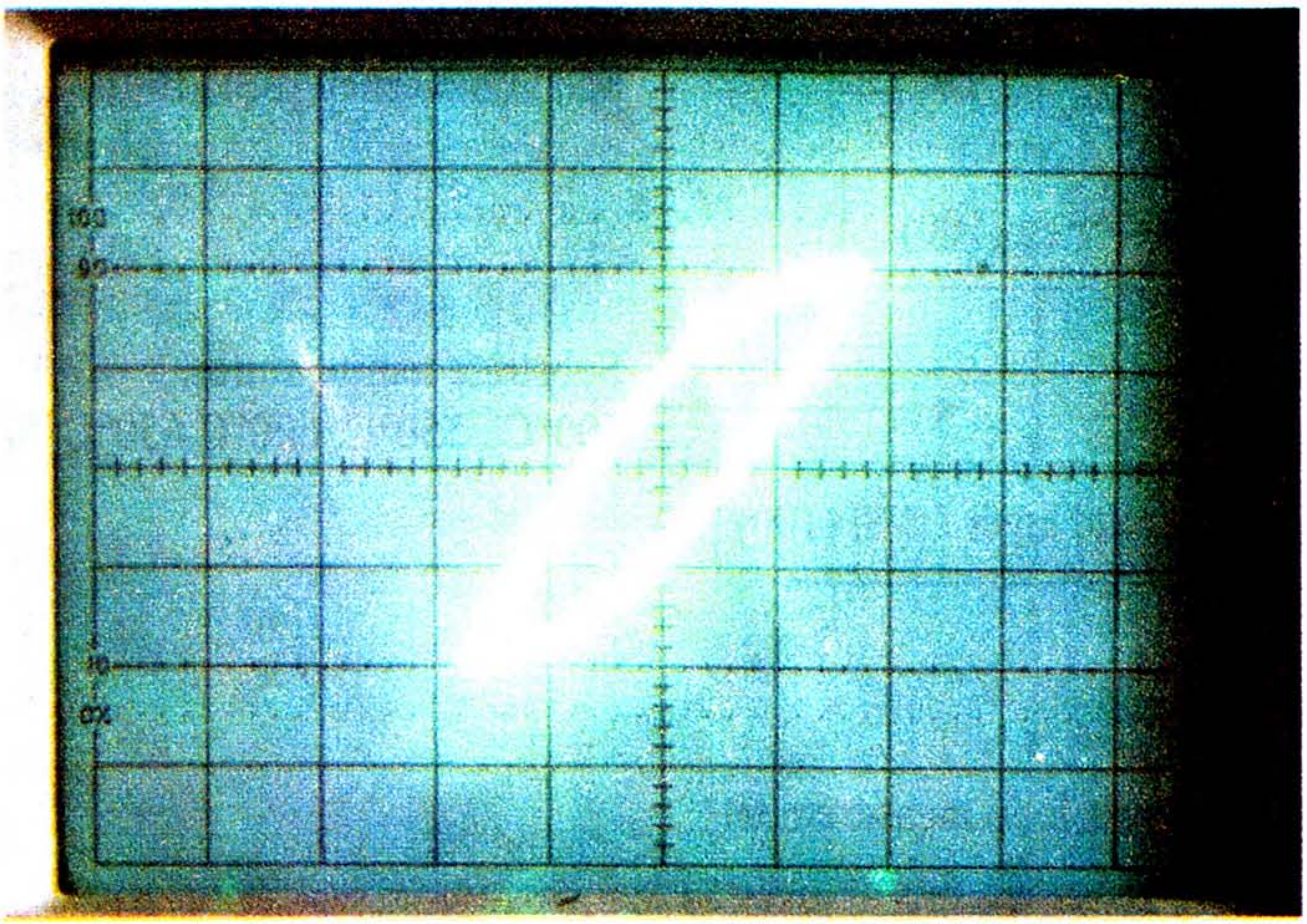

Fig. 3 (a) P-E hysteresis loop of $TiO_2$ thin film capacitor deposited on $SiO_2$ formed at 500°C

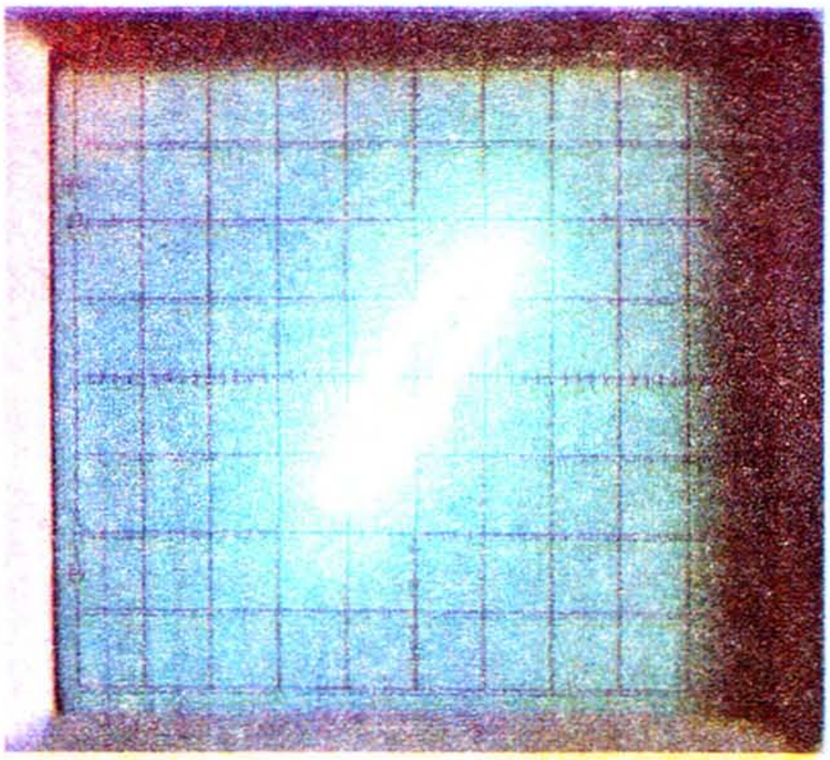

Fig. 3 (b) P-E hysteresis loop of $TiO_2$ thin film capacitor deposited on $SiO_2$ formed at 550 °C

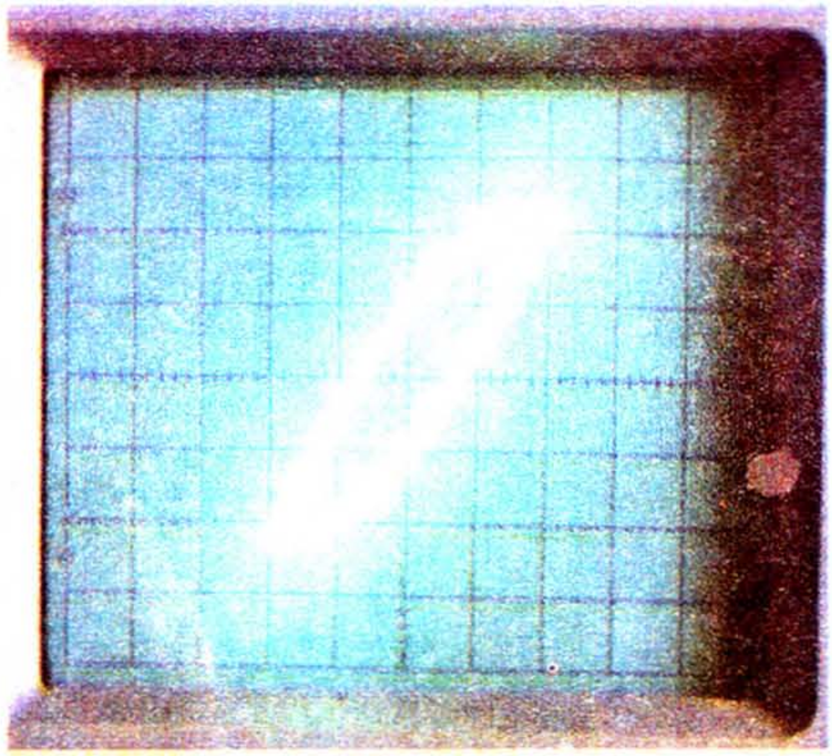

Fig. 3(c) P-E hysteresis loop of film capacitor deposited on $SiO_2$ formed at 600 °C

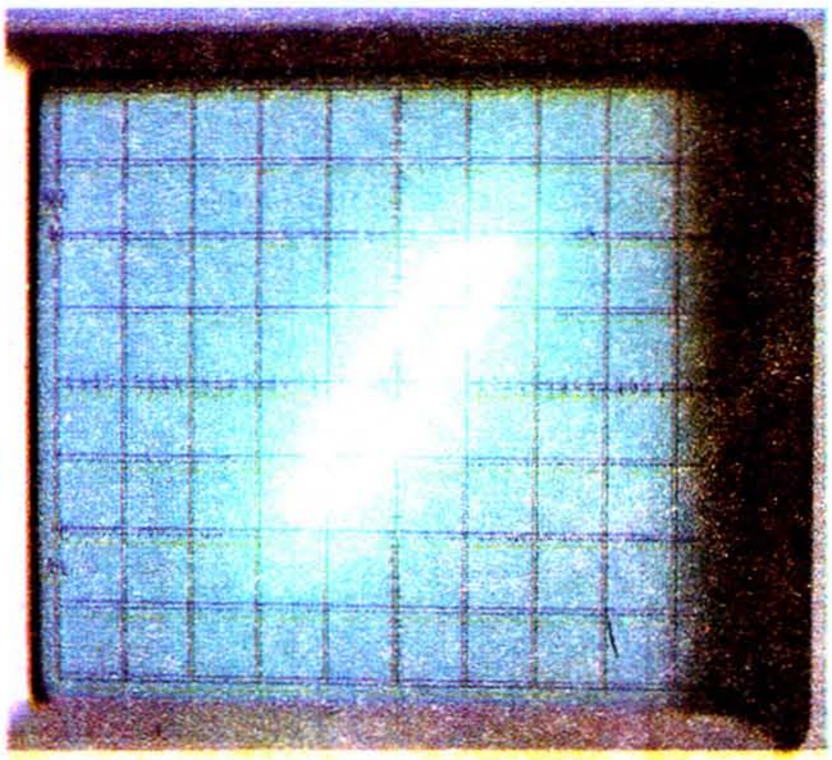

Fig. 3(d) P-E hysteresis loop of $TiO_2$ thin film capacitor deposited on $SiO_2$ formed at 650°C

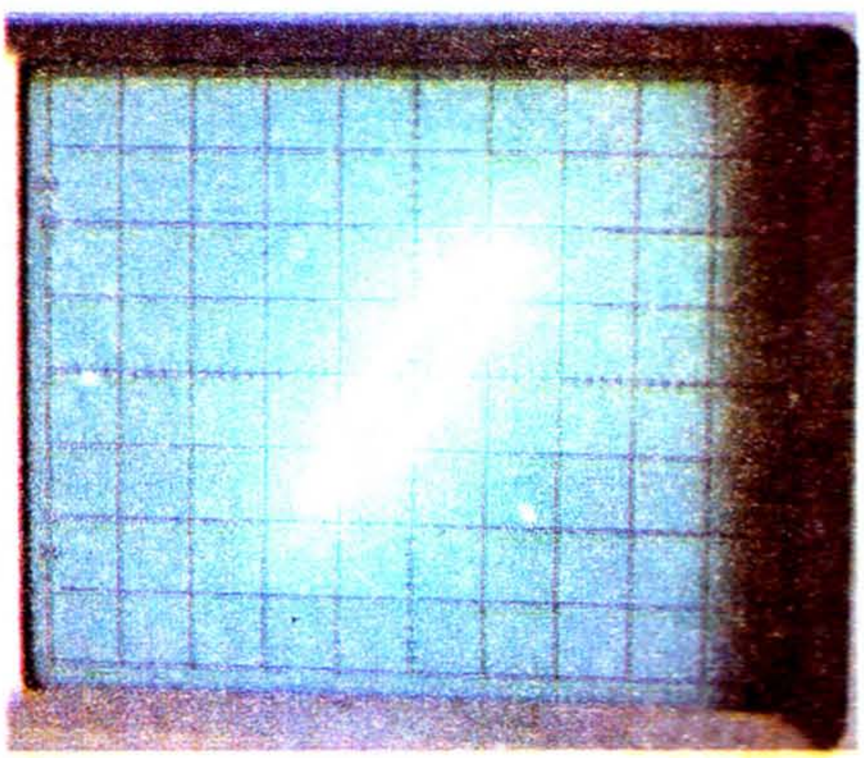

Fig. 3(e) P-E hysteresis loop of $TiO_2$ thin film capacitor deposited on $SiO_2$ formed at 700°C

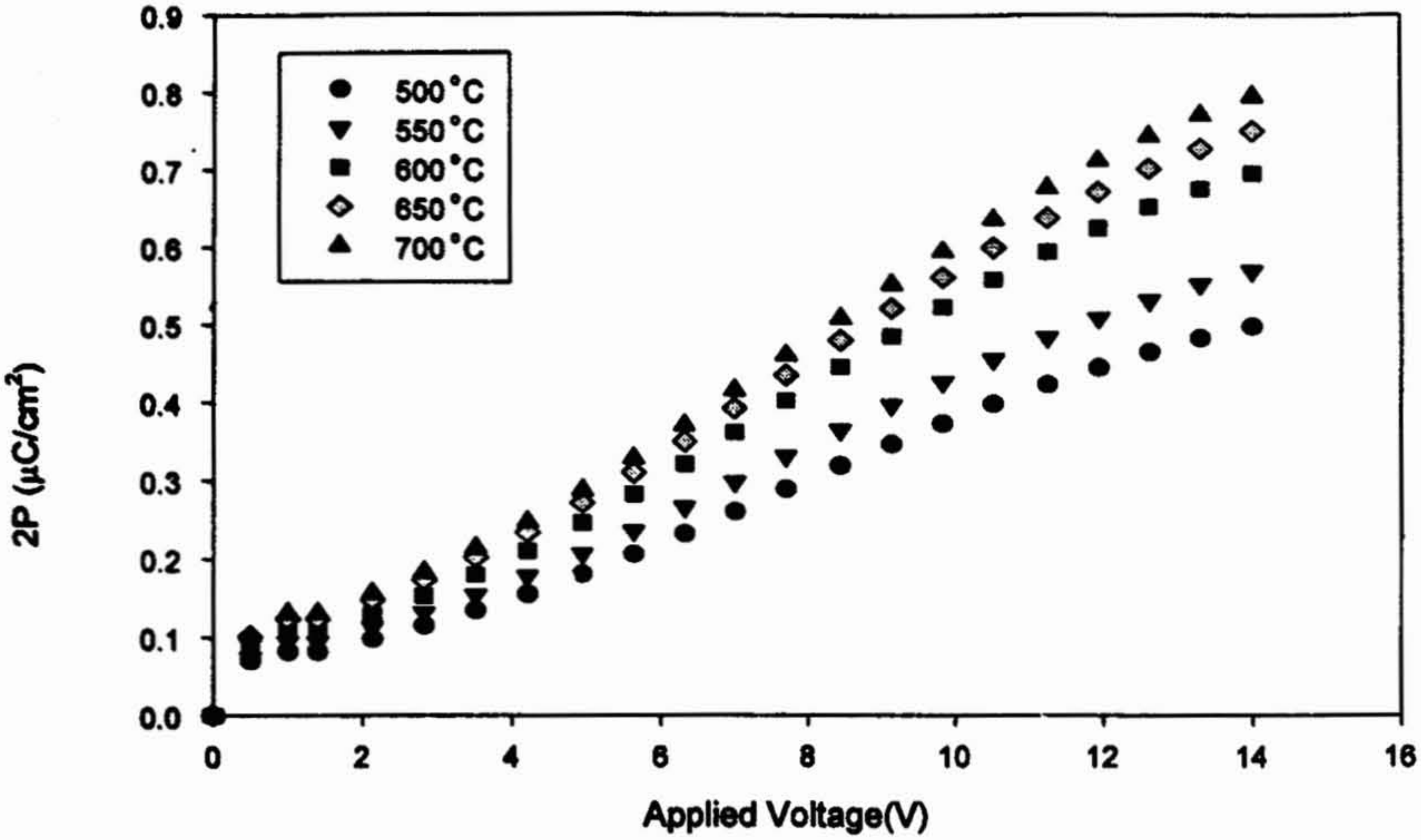


Fig. 4. Saturation properties of the $TiO_2$ /$SiO_2$ /p-Si thin film at various process temperature

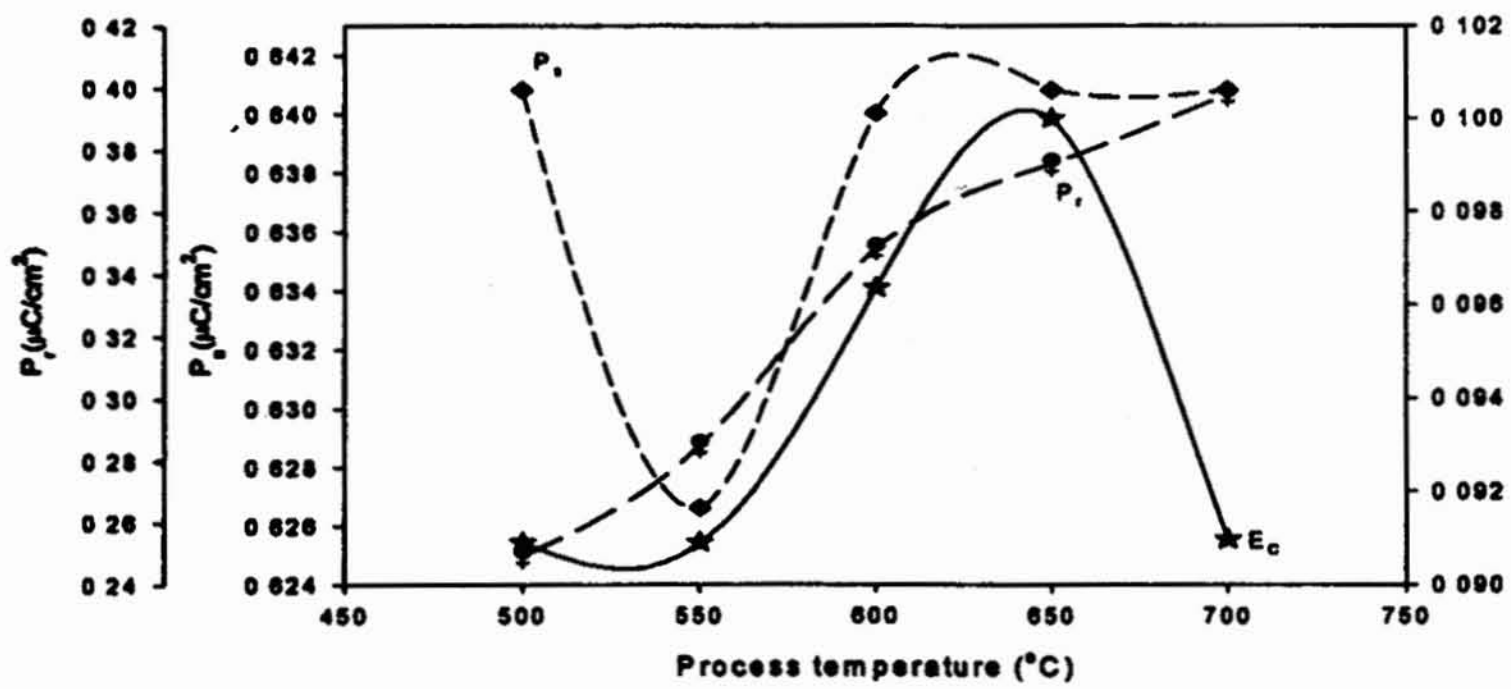


Fig. 5. Variation of $P_r$, $P_s$, $E_C$ of the $TiO_2$ /$SiO_2$ /p-Si thin film at various process temperature

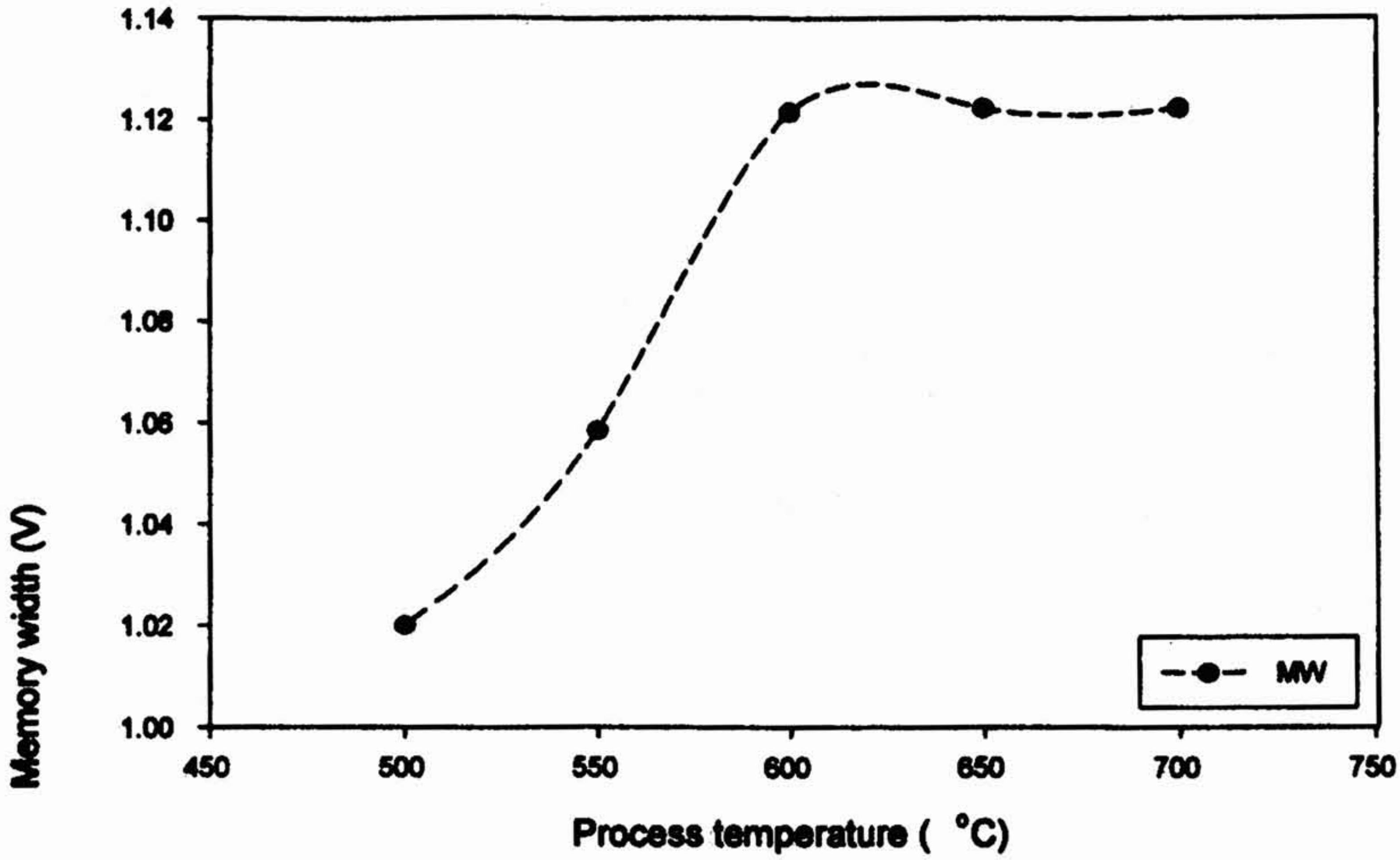


Fig. 6. Temperature dependence of the memory width of $TiO_2$ /$SiO_2$ /p-Si thin film

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